FLOATING GATE NON-VOLATILE MEMORY CELL WITH LOW ERASING VOLTAGE AND MANUFACTURING METHOD

Abstract of the Disclosure

A non-volatile memory cell of the type which includes at least one floating gate transistor and which is realized over a semiconductor substrate includes a source region, and a drain region, separated by a channel region which is overlaid by a thin layer of gate oxide. The gate oxide isolates a floating gate region from the substrate. The floating gate region is coupled to a control gate terminal. The floating gate region of the memory cell develops a first potential barrier between the semiconductor substrate and the gate oxide layer, and a second different potential barrier between the floating gate region and the gate oxide.